AMENDMENTS TO THE CLAIMS

Please **ADD** claim 11 as shown below.

Please **AMEND** claims 1-10 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A thin film transistor (TFT) array substrate for a liquid crystal display, comprising:

an insulating substrate including a display area and a peripheral area surrounding the display area, the peripheral area including ~~an upper~~ a first peripheral region arranged along a first edge of ~~above~~ the display area and a ~~lower~~ second peripheral region arranged ~~below~~ along a second edge of the display area;

a plurality of signal lines formed on the insulating substrate~~, wherein the signal lines are bundled~~ and divided into a plurality of blocks, each block including a predetermined number of signal lines;

a plurality of first ~~upper~~ repair lines formed in the ~~upper~~ first peripheral region, each crossing the signal lines of ~~the substrate, wherein the plurality of first upper repair lines cross~~ one or more of the plurality of blocks;

a ~~plurality of~~ second ~~upper~~ repair ~~lines~~ line formed in the ~~upper~~ first peripheral region and crossing ~~of the substrate, wherein the second upper repair lines cross~~ all of the plurality of signal lines;

a plurality of ~~first lower~~ third repair lines formed ~~at~~ in the ~~lower~~ second peripheral region and ~~of the substrate,~~ connected to the ~~corresponding~~ first ~~upper~~ repair lines corresponding thereto, wherein ~~the first lower~~ each third repair ~~lines cross~~ line crosses the signal lines crossed by the corresponding first upper repair line ~~lines~~; and

a ~~plurality of second lower~~ fourth repair ~~lines~~ line formed ~~at~~ in the ~~lower~~ second peripheral region ~~of the substrate, wherein the plurality of second lower repair lines cross~~ and crossing all of the plurality of signal lines~~;~~

~~a plurality of upper connection members crossing the first upper repair lines and the second upper repair lines; and~~

~~a plurality of lower connection members crossing the first lower repair lines and the second lower repair lines~~.

2. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim ~~1~~ 11, further comprising~~:~~ a plurality of first interconnection lines, each interconnecting the first ~~upper~~ repair ~~lines~~ line and the ~~first lower~~ third repair ~~lines~~ line corresponding thereto.

3. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 2, wherein ~~the~~ each first repair line ~~upper repair lines extend from~~ is connected to ~~two or more dummy pins of~~ an integrated ~~circuits~~ circuit for driving the signal lines~~,~~ and ~~are~~ coupled to the first interconnection ~~lines~~ line.

4. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 2, further comprising~~:~~ a plurality of second interconnection lines, each interconnecting the first ~~upper~~ repair ~~lines~~ line and the ~~first lower~~ third repair ~~lines~~ line corresponding thereto.

5. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim ~~1~~ 11, further comprising:

a ~~plurality of third upper~~ fifth repair ~~lines~~ line formed ~~at~~ in the ~~upper~~ first peripheral region ~~of the substrate while~~ and crossing the ~~upper~~ first connection members and all of the plurality of signal lines; and

a ~~plurality of third lower~~ sixth repair ~~lines~~ line formed ~~at~~ in the ~~lower~~ second peripheral region ~~of the substrate while~~ and crossing the ~~lower~~ second connection members and all of the plurality of signal lines.

6. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim ~~1~~ 11, wherein ~~each block of~~ the signal lines of each block are ~~comprises the signal lines~~ connected to an integrated circuit.

7. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 6, wherein the first ~~upper~~ line and the ~~first lower~~ third repair line cross ~~two blocks of~~ the signal lines of two neighboring blocks.

8. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 7, wherein ~~one or more of~~ the ~~upper~~ first connection member and the ~~lower~~ second connection member are ~~formed at~~ provided in each block ~~of the signal lines~~.

9. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 4, wherein the first interconnection line and the second interconnection line are formed on a printed circuit board.

10. (Currently Amended) The ~~thin film transistor~~ TFT array substrate of claim 4, further comprising~~:~~ a signal amplifying circuit provided in the first interconnection line and the second interconnection line.

11. (New) The TFT array substrate of claim 1, further comprising:

a plurality of first connection members, each crossing the first repair line and the second repair line; and

a plurality of second connection members, each crossing the third repair line and the fourth repair line.